holes being self aligned to said outer edges of said spacer oxide layer.

15. (Clean) In a vertically integrated nonvolatile memory cell structure formed using a vertical well that penetrates doped drain and channel regions and into a source region of a substrate, said vertical well having a top edge and a bottom, a self aligned floating gate insulating layer substructure comprising:

a self aligned floating gate insulating material layer on all vertical walls of said well and which does not extend above the top of said well; and

an insulating layer on the bottom of said well.

16. (Clean) The self aligned floating gate insulating material substructure of claim 15 manufactured by a process which does not use any critical mask in the steps used to form said self aligned floating gate insulating material layer such that it does not extend above said top of said well , where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit.

REMARKS

In the interview with Examiner Crane on December 6, 2002, the Examiner asked for more argument why the claimed invention distinguishes over the Otani et al. reference (US 5,786,612) Figure 33.

The applicant will distinguish Otani et al. (5,786,612) on the basis of structural differences without admitting it is prior art. In particular, the applicant hereby makes an offer of proof that if the Examiner does not for some reason accept the fact that there are significant structural differences over Otani et al., the applicant reserves the right to file a Rule 131 declaration swearing behind Otani et al. which was filed just two months before the filing date of the application at bar.

OTANI'S FLOATING GATE IS NOT SELF ALIGNED BECAUSE IT USES A CRITICAL MASK

One reason the claimed invention distinguishes over the Otani et al. reference is that the Otani et al. floating gates 20 in the embodiments represented by Figures 24 and 33 are not self aligned to cover **all** vertical surfaces of the well (the well is 3 in Figure 24 and 27 in Figure 33). This is because the Otani et al. patent teaches that photolithography and etching techniques are used to form the floating gate 20 and the gate insulating layer 19. This means that a mask is used to form the floating gate 20 so as to cover only one vertical surface of the well, and therefore the Otani et al. floating gate will not be self aligned to cover **all** vertical surfaces of the well because it requires a critical mask to make it cover just one wall of the well. Specifically, at Col. 13, line 65 to Col. 14, lines 1-10 (as to Figure 33) and Col. 12, lines 1-11 (as to Figure 24) Otani et al. teach:

> **After that, as shown in Figure 30, the polycrystalline polysilicon layer and the like are processed by means of the photolithographic technique and the etching technique to have the desired patterns, thus obtaining the gate oxide films 19 and the floating gate electrode 20.**

Emphasis added

An identical teachings is given at Col. 13 and 14 with respect to the embodiment of Figure 33.

The critical mask needed in the Otani et al. process to form the floating gate is an etch mask to etch away the poly from all the walls except one of the Otani well. This etch mask is shown at EM in the mark up of Otani's Figure 13 in Figure A-1 of Exhibit A attached hereto. This etch mask EM is a critical mask and it must be very precisely aligned to have an edge down the middle of the well. This is very difficult to do with a well that is only 0.6 microns wide (which was the achievable feature size when our patent application was filed) and may be impossible to achieve with today's much smaller feature sizes. A registration error too far to the right in Figure A-1 would possibly lead to the wet etch taking out all the poly of layer 7A on the wall of the well where the floating gate was supposed to be rendering the device inoperative. A registration error too far to the left in Figure A-1 could lead to floating gate poly on all walls of the well with no room left for the control gate poly thereby rendering the device inoperative.

IMPOSSIBILITY OF THE OTANI STRUCTURE IS HIGHLY LIKELY

It is highly likely that the result of Otani's Figure 14 could not be achieved with a feature size of 0.6 microns for the width of the well. This is because with a well that 0.6 micron narrow, the actual result of the deposition of the poly layer 7A for the floating gate would fill the well thereby messing up the etch mask operation to remove the floating gate poly from all walls of the Otani well except one. Figure A-2 is a drawing to scale of the Otani well structure after the floating gate poly has been deposited and an etch mask EM have been formed and perfectly aligned using the dimensions taught in the Otani patent. The insulating oxide under the floating gate poly is so thin, it is not shown at all. Figure A-2 assumes the alignment of the etch mask EM to the tiny space between the poly walls could actually be achieved, which we submit with a 0.6 micron wide trench (Col. 9, line 44 of Otani et al.) with a 200 nanometer thick poly layer 7A deposited on both walls, the space between the poly walls would be too small to successfully align the etch mask EM. The dashed line 100 in Figure A-2 represents the etch line of the wet etch when the poly layer 7A is etched away to remove the poly from the walls of the well except under the etch mask EM. This etch line shows how the poly is eaten away under the etch mask and could adversely affect the performance of the device since floating gate might not completely cover the channel.

These technical difficulties or impossibilty in building the Otani et al. structure teach away from the invention and would discourage one skilled in the art from attempting to combine the teachings of Otani et al. with the other references in the obviousness rejection combination.

THE CORRECT INTERPRETATION OF THE LIMITATION "SELF ALIGNED"

The correct interpretation of the limitation "self aligned" in the claims as used with respect to either the floating gate or its underlying gate oxide layer or the contacts to the drain is that the structure that is said to be self aligned is that the structure has the characteristics which inherently result from the fact that it is made without using a critical mask. A critical mask is defined as a mask which must be tightly aligned to another structure

on the same of or a different layer such as the etch mask EM in Figures A-2 of Exhibit A. Self alignment of a structure has structural ramifications which are different for different structures but which always result in a smaller total cell area. For example, the structural result of self alignment of the floating gate poly in the claimed invention (or its underlying gate oxide layer which also is self aligned) is that the floating gate poly and its gate oxide layer separating the floating date from the channel always cover all walls of the well and will never stick out past the edge of the well or have any horizontal component on the surface of the substrate or in the bottom of the well. This makes the cell size smaller because there is no need to space the bit line contact hole to the drain 14 in Figure 5 farther away from the edge of the well to account for registration errors of a critical mask to form the floating gate 22 because there is no critical mask. Therefore, there never will be registration errors, and the cell can be made smaller because there is no need to provide a safety cushion around the area where the mask to form the floating gate is supposed to be registered for purposes of positioning the drain contact area.

In other words, the cell of the invention is smaller because no critical mask is needed in the process to form the floating gate in the cell of the invention to define the extents of the floating gate electrode or its underlying gate oxide layer. This is because an anisotropic etch is used to remove the horizontal components of the floating gate poly and leave floating gate poly only on all vertical surfaces of the well. If a mask were used in the invention, registration errors would means that the floating gate poly could sometimes have a horizontal component on the top of the surface of the substrate. If the invention required a mask to form the floating gate, it would mean that the bit line contacts to the drain would have to be spaced further away from the edge of the well to provide a safety margin for these floating gate mask misalignments. The resulting cell of the invention is shown in plan view in Figure 6 of the patent application at bar and this figure is repeated with markups as Figure A-5 of Exhibit A. This figure shows that the horizontal distance from the edge of one cell 106 to the same edge 108 of the next cell is only 2F where F is the minimum possible feature size or linewidth.

Likewise, the vertical distance from the edge 110 of one cell to the same edge 112 of the next cell is 2F. The total area of each cell of the claimed invention is therefore $4F^2$.

There are only four masks needed to form the nonvolatile memory cell of the invention, and none of them are critical in alignment. These four masks are illustrated in Figure A-6 of Exhibit A. Note that the bit line mask forms a continuous bit line that passes over each cell and makes contact with shared drain areas 114 and 116 in Figure A-6 through self aligned bit line contact holes. This bit line is shown at 30 in Figure A-7 of Exhibit A which shows the completed device of the invention and corresponds to Figure 5 of the patent application at bar. The self aligned contact holes are shown at 118 and 120 in Figure A-7, and the shared drain areas 114 and 116 correspond to drain areas 14 in Figure A-7 on both sides of the well. The drain region actually exists on two sides of the well. Those two sides are the sides of the well which are orthogonal to the long axis of the row (which is the long axis of the bit line). However, the self aligned contact holes for the bit line to make contacts to the drain regions only exist on the same row of cells and this causes drain regions to be shared between cells on the same row only and prevents the drain regions from being shared between neighboring cells in the same column.

The fact that the floating gate poly of the claimed invention (22 in Figure 5) is self aligned and on <u>all</u> vertical surfaces of the well and not on just one surface as in Otani has at least two hugely significant effects on the overall cell area in the invention. Both of these factors make the non volatile memory cell of the invention (see Figures 5 and 6) much smaller in area ($4F^2$ where F is the minimum feature size otherwise known as the line width) than Otani et al. ($12F^2$ for first embodiment and $8F^2$ for second embodiment - See Figure 23) or the best available prior art from Samsung ($10F^2$).

First, the self aligned floating gate in the invention is made without a mask and will never suffer damage from misalignment of a mask and will never have a horizontal component on the top of the well caused by misregistration of a mask. This means that the

self aligned contact holes to the drain regions can be placed closer to the wells than they can be placed in Otani et al. because there is no safey cushion of space between the drain contact and the well that is necessary to prevent errors in device construction caused by misalignment of a mask. Otani et al. teach the use of at least 6 masks to get to the final device structure, and there are 5 critical mask alignments necessary.

The first critical alignment in the Otani process is between the well and the isolation field oxide and requires precise registration of the mask to form the wells between the isolation oxide regions.

The second critical alignment required in Otani et al. is in the alignment of the mask to form the etch mask to go down into each well and protect the floating gate poly on one wall of the well only and etch away the rest of the floating gate poly. That is the masking step between Figure 13 and Figure 14 and the counterpart steps for the second and third embodiments represented by Figures 22 and 33.

The third critical alignment in Otani is the mask to form the control gate in the trench portion where the floating gate poly has been etched away. This critical alignment of mask 5 happens between Figures 16 and 17 in Otani et al. and the counterpart steps in the second and third embodiments.

Another alignment (non critical) in Otani is to define the N+ implant regions for the drain implant. This alignment step if for mask 6 and happens between Figures 17 and 18 and their counterpart figures for the second and third embodiments.

The fourth critical alignment required by Otani et al. is the to form the contact to the second poly of the control gate.

The last critical alignment required by Otani et al. is to form the contact window for the metal to drain contact to form the bit line contacts to each cell.

The result of all these masks and critical alignments is the cell of Figure 23 (Figure A-8 of Exhibit A) for the second embodiment and Figure 1 for the first embodimet. Figure A-8 is marked up with the dimensions of one cell in the horizontal and vertical directions expressed

in terms of the minimum feature size F. The square area of the smaller second embodiment of Figure 24 is $8F^2$ as opposed to the $4F^2$ size of the cell of the invention shown in Figure A-5 of Exhibit A. Note that in the Otani et al. cell of Figure A-8 of Exhibit A, the drain area (under contact window 14) is shared only between cells in every other column because the drain is not on both sides of every trench but is on one side only. These asymetric structures are then faced to one another to share a contact hole and a drain but a cell in Otani et al. cannot share a drain and contact hole with its neighboring cells on both sides and is done in the cell of the invention. This is a major reason why the array of the invention is twice as dense as the Otani et al. array and is made possible by the annulus self aligned floating gate in claim 1 and the drain region which surrounds the well.

The self aligned floating gate annulus, the vertical orientation of the transistor, the shared drain and the self aligned contact windows to the drain regions are the main reasons why the cell of the invention is so small. All these features are expressed in limitations of claim 1, as amended herein.

OUR FLOATING GATE ANNULUS

The significance of the difference that the Otani et al. floating gate does not cover all vertical surfaces of the well whereas the floating gate of the claims (as amended herein) does cover all vertical surfaces of the well is that this allows sharing of a drain region between neighboring cells on both sides of each well in a row in the invention. This was explained above, and it has a huge impact on the cell size and makes the arrays of cells of the invention much more dense that the Otani et al. arrays. This feature is embodied in the limitations of the claims that require the self aligned floating gate to be on all the vertical walls of the well.

REMARKS AS TO AMENDMENTS TO CLAIM 1

The amendments to claim 1 to distinguish over Otani et al. are marked in bold and underlined. All other changes to the claim were voluntary and improve the form of the claim. For example, the fact that the word line also functions as the control gate was added to

make this clear. The changes in bold have significance and render the claim patentable for the reasons given above. The self aligned limitation to the bit line was added because the bit line contact hole to the drain area is not formed with a critical mask and has its inner edge (the edge closest to the well) established by the outer edge of the spacer layer of oxide 32 and 32' in Figure 5. Otani et al. form their contact hole 14 to the drain 11 using a mask. This means the contact hole must be spaced far enough away from the wells per the design rules to allow for misregistration of the contact hole mask. This makes the Otani et al. cell larger in area than the cell of the invention. The spacer insulating layer limitation was added to add missing structure needed to define a self aligned bit line which contacts the drain region through a contact hole the inner edge of which is defined by the spacer layer.

Claim 1 would be patentable over Otani et al. even if Otani et al. was prior art because of the self aligned floating gate annulus which allows drain regions on both sides of each well to be shared between neighboring cells on the same row. Note that claim 1 calls for the drain region to be on both sides of the well that are orthogonal to the long axis of the bit line and calls for the bit line to make contact to the drain region through a self aligned contact hole. This means drain regions on both sides of the well in the same row and which share a bit line can be shared between neighboring cells on both sides of each well in the same row. This allows a much denser array to be formed than the Otani et al. cell where the drain region is only on one side of the well (the same side as the floating gate) and which is contacted by the bit line through a contact hole which is formed with a mask.

REMARKS AS TO CHANGES TO CLAIM 2

Claim 2 was amended to specify that the well has a drain region on two sides (the two sides orthogonal to the long axis of the bit line) and has also be amended to specify that the floating gate is formed on all walls of said well. This distinguishes over Otani et al. by the floating gate annulus and the drain surrounding the well.

REMARKS AS TO CHANGES TO CLAIM 3

The changes in bold reflect the changes that were made to futher distinguish the

invention from Otani et al.. The claim was changed into an array claim so as to be able to claim the shared drain regions of each side of each well of a nonvolatile memory cell in a row. The floating gate clause was amended to specifically recite that it is an annulus. Further, the self aligned nature of the drain contacts was claimed by defining the exact structures of the spacer insulating layer which defines the inner edge of the self aligned drain contact window and by defining that the bit line passes over each nonvolatile memory cell in the array and fills the self aligned drain contact windows on each side of the well in the same row. Shared drain regions and drain contacts can be implemented because only one memory cell is activated at any particular time in the array so it never happens that two memory cells sharing the same drain region are both being read or written to simultaneously.

REMARKS AS TO CHANGES TO CLAIM 4

The changes to claim 4 were made voluntarily to more clearly specify that the bit lines are above the top surface of the substrate, pass over the top of each word line and contact the shared drain regions at all points between the outer edges of the spacer layers that insulate the side walls of adjacent word lines.

Changes to all the new claims are to conform them to these remarks and more clearly distinguish them from the Otani et al. reference which does not teach self aligned floating gates formed without using a critical mask so as to cover all the vertical walls of the well.

Attached hereto is the declaration of Madhu Vora and Exhibit 1 thereto which supply evidence in support of the above detailed arguments and point out graphically why the mask used to define the word line in the Vora cell is not critical and how misaslignment of this mask will not destroy the resulting Vora cell.

Respectfully submitted,

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APPENDIX

1. [Thrice Amended-Version to show changes] A nonvolatile EPROM or EEPROM memory cell formed using a vertical MOS transistor comprising:

a semiconductor substrate doped to have a first conductivity type so as to act as a source region of said nonvolatile memory cell, said first conductivity type being either N-type or P-type, and having a top surface which extends laterally and a depth which extends vertically;

a vertical MOS transistor formed by alternating, abutting N-type and P-type doped layers in said substrate which have junctions therebetween to form a channel region and a drain region of said vertical MOS transistor with said drain region having said first conductivity type and said channel region having a second conductivity type which is P-type if said first conductivity type is N-type and is N-type if said first conductivity type is P-type, said substrate forming a source region of said first conductivity type of said vertical MOS transistor, said source regions having a junction with said channel region, and wherein a well with one or more walls is etched vertically into said substrate through said channel and drain regions and at least partially into said source region such that said drain [and channel regions surround] exists on at least two sides said well and forms at least a portion of [said one or more] at least two walls of said well, said well having a floating gate of conductive material formed therein which is self aligned to not extend laterally beyond edges of said well ***and covers all vertical surfaces of said well***, said edges of said well being defined by said one or more walls of said well, and said self aligned floating gate insulated from said channel and drain regions and said substrate by a self aligned layer of insulating material, said floating gate being laterally adjacent to at least said portion of said wall of said well formed by said channel region of said vertical MOS transistor such that differing levels of trapped charge in said floating gate affects the conductivity of said channel region and a threshold of said nonvolatile memory cell in the form of a vertical MOS transistor;

a word line contact which also functions as a control gate of said nonvolatile memory cell comprising a layer of conductive material formed on said substrate so as to extend vertically down into said well and lie laterally adjacent to said floating gate but be insulated therefrom by an insulation layer such that voltage applied to said control gate affects the charge on said floating gate; [and]

a spacer insulating layer formed on top and side surfaces of said word line contact, with an edge of said spacer insulating layer defining an inner edge of a contact hole to said drain region, said inner edge being an edge of said contact hole closest to said well; and

a **self aligned** bit line and contact to the drain area of said vertical MOS transistor, said self aligned bit line comprising a layer of conductive material formed on said substrate so as to be in electrical contact with said drain regions on two sides of said well of said vertical MOS transistor **via self aligned contact holes**.

2. [Thrice Amended-Version to show changes] A substructure of a vertical MOS transistor forming part of a nonvolatile memory cell comprising:

a semiconductor substrate having a top surface which extends in a lateral direction and a thickness which extends in a vertical direction and having a drain region of a first conductivity type formed therein and suitable to act as a drain of a vertical MOS transistor;

a buried layer channel region in said semiconductor substrate doped so as to have a second conductivity type having the majority of charge carriers therein of a different polarity than said first conductivity type and suitable to act as a channel of a vertical MOS transistor formed in said substrate;

a source region of said semiconductor substrate below said channel region, said source region being doped so as to have said first conductivity type and suitable to act as a source of a vertical MOS transistor;

a well etched vertically into said semiconductor substrate, said well having one or more side walls and being deep enough to penetrate through said drain region and channel region such that said drain region and said channel region are on two sides of said well and[, said channel region] and said well extending at least partially into said source region such that at least some portions of said one or more [side] walls of said well are defined by intersections with said source, drain and channel regions;

an ~~insulating layer~~ covering the bottom of said well;

a gate insulating layer formed on said one or more sidewalls of said well;

a self aligned floating gate formed without using any critical mask comprising a conductive material formed within said well on said gate insulating layer on each wall of said well but formed so as to not extend beyond said one or more walls of said well and positioned laterally adjacent to the intersection of said one or more side walls and said channel region such that trapped charge in said floating gate affect the conductivity of said channel regions and a threshold of said vertical MOS transistor, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit;

an insulating layer formed over said self aligned floating gate so as to electrically isolate said floating gate from all surrounding structures; and

a word line comprising conductive material deposited so as to extend into said well far enough to lie laterally adjacent to said floating gate so as to form a control gate of a vertical MOS transistor nonvolatile EEPROM or EPROM memory cell structure.

3. [Thrice Amended-Version to show changes] A nonvolatile memory cell array comprising:

a semiconductor substrate having a top surface which extends laterally and having a depth which extends vertically;

an array of nonvolatile memory cells arranged as a plurality of nonvolatile memory cells arranged into rows having a longest axis along which said nonvolatile memory cells are spaced and columns having a long axis along which said nonvolatile memory cells are spaced, and wherein each nonvolatile memory cell in each row shares a common drain region with a neighboring memory cell to the left in said row and shares a common drain region with a neighboring memory cell to the right in said row, and wherein each drain region in each row is contacted by a bit line through a self aligned contact window, and wherein each memory cell in a column shares a word line which also acts as a control gate at the location of each memory cell, and wherein each said nonvolatile memory cell in said array is comprised of:

a nonvolatile EEPROM or EPROM memory cell which is formed using a vertical MOS transistor (hereafter just referred to as a vertical MOS transistor or nonvolatile memory cell), comprising:

a vertical MOS transistor formed by a first layer of said substrate of N-type conductivity forming a drain region of said vertical MOS transistor, a second layer of said substrate of P-type conductivity and vertically adjacent to and beneath said first layer relative to said top surface of said substrate so as to form a channel region of said vertical MOS transistor, and a third layer of said substrate of N-type conductivity within said substrate and vertically adjacent to and beneath said second layer relative to said top surface of said substrate so as to form a source region of said vertical MOS transistor, said substrate also having a well vertically etched therein so as to penetrate through said first and second layers and at least partially through said third layer **such that said well has a drain region on at least two sides thereof, said drain regions being**

under said bit line of the row in which said vertical MOS transistor is formed, said well having at least a portion of the wall or walls thereof formed by the intersection of said well with said drain and channel regions, and ***said well having a floating gate of conductive material formed therein which is self aligned by virtue of having been formed without the use of a critical mask so as to form an annulus with conductive material of said floating gate on each vertical wall of said well and formed so as to not extend laterally beyond the wall or walls of said well***, said floating gate including at least a portion thereof which lies laterally adjacent to said portion of said wall or walls of said well formed by the intersection of said well with said channel region such that trapped charge in said floating gate affects the conductivity of said channel regions and a threshold of said vertical MOS transistor, said floating gate being insulated by a layer of gate insulating material from said first, second and third layers, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit;

a portion of said word line acting as a control gate of said nonvolatile memory cell, said control gate comprising a layer of conductive material formed so as to extend down into said well and have at least a portion thereof which is laterally adjacent to said floating gate but insulated therefrom by an insulation layer so as to act as [a] said control gate for said vertical MOS transistor;

a self aligned drain contact formed from a portion of said bit line for a row of said array in which said vertical MOS transistor is formed, said bit line comprising a layer of conductive material formed above said top surface of said substrate **and passing over each said nonvolatile memory cell in said row of said array in which said nonvolatile memory cell is formed and filling self aligned drain contact windows on each side of said well in a row of which said vertical MOS transistor is a part so as to be in electrical contact with said shared drain regions of each side of said well in a row of which said vertical MOS transistor is a part;** [a portion of said first layer;] and

a spacer layer of insulating material insulating said word line from said bit line **and wherein portions of said spacer layer insulating outer edges of said word line which forms a control gate of said nonvolatile memory cell define the inner edge of said self aligned drain contact window on each side of said well in a row of which said nonvolatile memory cell is a part, said inner edge of said self aligned contact windows being defined as the edges closest to said well, and wherein said outer edges of said word line are defined as edges of said word line farthest from a center of said well along said longest axis of a row of said array of which said nonvolatile memory cell is a part**.

4. [Amended-Version to show changes] The apparatus of claim 3 wherein said [memory cell is part of an array comprised of rows and columns of adjacent memory cells and wherein said] bit line is formed above said first layer so as to be above the top surface of said substrate and passes over said word lines at the location of each said nonvolatile memory cell and wherein said self aligned contact windows extend from said outer edge of each word line to the closest outer edge of an adjacent word line, where an adjacent word line is

defined as a word line in an immediately adjacent column of said array, the structure of said self aligned drain contact windows thereby being such that each said bit line of a row of said array contacts each [contacts] said first layer shared drain region at all points that form a top surface of said first layer between said spacer layers of insulating material that [insulates the] insulate said outer edges of said adjacent word lines[of adjacent memory cells].

Please add a new claim 7 as follows (these claims were added and paid for in the first response to this office action and are repeated here for convenience and may be amended as marked in the appendix):

7. [Once Amended-Version to show changes] A vertically integrated nonvolatile memory MOS transistor formed along a long axis of a row of nonvolatile memory transistors in a memory array, comprising:

a substrate having a top surface that extends horizontally and a depth which extends vertically and which is doped to a have a first conductivity type and having an active area therein doped to a second conductivity type and a conductivity level suitable to act as a source region of a vertically integrated MOS [non volatile] nonvolatile memory transistor;

a buried channel region in said active area doped to have said first conductivity type and a conductivity suitable to act as a channel region of said vertically integrated MOS [non volatile] nonvolatile memory transistor;

a drain region in said active area doped to have said second conductivity type and a conductivity suitable to act as a drain region of said vertically integrated MOS [non volatile] nonvolatile memory transistor;

a well etched vertically down through said drain and channel regions and at least partially into said source region so as to have a drain region on at least two sides of said well which are orthogonal to said long axis;

an gate insulation layer formed on the walls of said well and an insulating layer on a floor of ~~said well~~;

a self aligned conductive floating gate formed on [the] all walls of said well without using any critical mask so as to form an annulus and formed so as to never extend outside said walls of said well and formed on said gate insulation ~~layer such that~~ all portions of the walls of ~~said well that intersect said channel region~~ are horizontally adjacent said floating gate such that trapped charge on said floating gate can alter the conductivity of ~~said channel region and the threshold of said~~ vertically integrated MOS [non volatile] nonvolatile memory transistor, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit;

~~an intergate insulation layer formed on said floating gate suitable to insulate~~ said floating gate from all surrounding conductive structures;

a conductive control gate formed in said well so as to be horizontally adjacent to said floating gate such that a first potential applied to said control gate causes charges to tunnel into said floating gate and a second potential applied to said control gate causes charges to tunnel out of said floating gate, said control gate extending up to and making contact with or being part of a conductive word line formed across said top surface of said substrate;

a control gate insulating layer which insulates the top of said word line and one or more spacer insulation layers which insulate the sides of said word line the outer edges of said spacer insulation layer defining the inner edges of a self aligned contact hole to said drain region on each side of said well along said long axis of said row of said nonvolatile memory transistors in an array, said outer edges being defined as the edges farthest from the center line of said well in a direction along said long axis of said row;

[one or more] two self aligned contact windows which are etched so as to be

self aligned to [the] said outer edges of said spacer insulation layers and which open said drain region to electrical contact on each side of said well along said long axis of said row; and

a conductive bit line formed across said top surface of said substrate along said long axis of said row so as to make contact with said drain region through each of said [one or more] two self aligned contact windows.

8. The apparatus of claim 1 wherein said N-type and P-typed doped layers in said substrate forming said channel region and said drain regions are formed without using any mask or only using non critical masks where non critical masks are defined as masks which are used to do only very loose alignment between layers.

9. [Once Amended-Version To Show Changes] The apparatus of claim 1 wherein said nonvolatile memory cell is formed with a process which simultaneously forms PMOS and NMOS devices on the same substrate as said nonvolatile memory cell but forms said PMOS and NMOS devices in different active areas from an active area in which said nonvolatile memory cell is formed, and wherein said source, channel and drain regions of said [non volatile] nonvolatile memory cell are formed with said process which simultaneously forms said PMOS and NMOS devices and are formed while said active areas of said PMOS and NMOS devices are covered by an insulation layer.

10. [Once Amended-Version To Show Changes] In a vertically integrated nonvolatile memory cell structure formed using a vertical well that penetrates doped drain and channel regions and into a source region of a substrate such that said doped drain and channel regions are adjacent to at least two sides of said well, said two sides being sides orthogonal to a long axis of a row of nonvolatile memory cells in an array of nonvolatile memory cells of which said vertically integrated nonvolatile memory cell structure is a part, said vertical well having a top edge defined by the intersection of vertical walls of said well with a top surface of said drain region and having a bottom, [said] a self aligned floating gate substructure comprising:

a self aligned floating gate insulating material layer on said [the] vertical walls of said well which does not ever extend above said top edge of said well;

an insulating layer on said bottom of said well;

a self aligned floating gate conductor material formed on [the] said [layer of] self aligned floating gate insulating material so as to form an annulus that covers all vertical walls of said well as so as to not ever extend above said top edge of said vertical well, said self aligned floating gate conductor material formed without using a critical mask, , where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit.

11. [Once Amended-Version to show changes] The apparatus of claim 10 further comprising a self aligned layer of silicon dioxide/nitride/silicon dioxide (hereafter ONO) covering said self aligned floating gate conductor material, and a doped polysilicon conductor control gate covering said ONO layer, said control gate [being self aligned to an edge of said floating gate at said bottom of said well but] extending above said top edge of said well, and a layer of silicon dioxide insulator covering a top surface of said control gate and self aligned spacer layers of silicon dioxide insulating [vertical] side edges of said control gate, said ONO layer being self aligned so as to not extend horizontally beyond [the] said side edges of said [spacer layers of silicon dioxide insulator and insulating said] control gate[from said floating gate].

12. The apparatus of claim 11 ***wherein said self aligned floating gate insulating***

material layer, said insulating layer on said bottom of said well, said self aligned floating gate conductor material, said self aligned control gate and said self aligned ONO layer all are formed without using a critical mask, , where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit [where a critical mask is defined as a mask which is required for tight tolerance alignment between different layers of a semiconductor structure].

13 . [Once Amended-Version to show changes] The apparatus of claim 10 wherein said self aligned floating gate substructure is formed by the following process:

forming a vertical well by etching vertically through a layer of silicon dioxide (herafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

anisotropically etching said nitride back from all horizontal surfaces to leave nitride only on said vertical walls of said well;

growing a layer of oxide on said bottom of said well;

wet etching said nitride off said vertical walls of said well to expose said pad oxide;

growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

depositing a layer of doped polysilicon over said substrate and into said well to cover said vertical walls and bottom of said well;

forming a self aligned floating gate without using a mask by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and said bottom of said vertical well and leaving doped polysilicon on all vertical walls of said well.

14. [Once Amended-Version to show changes] The apparatus of claim 11 wherein said self aligned floating gate substructure, said self aligned control gate and said self aligned ONO layer are formed by the following process:

1) forming a vertical well by etching vertically through a layer of silicon dioxide (herafter oxide) covering a top surface of said substrate of semiconductor material, and etching vertically down into said substrate through said doped drain and channel regions and into said source region;

2) depositing a layer of nitride insulator on the bottom of said well and on pad oxide formed on vertical side walls of said well and on horizontal surfaces of an insulating layer over said drain region;

3) anisotropically etching said nitride back from all horizontal surfaces to leave nitride only on said vertical walls of said well;

4) growing a layer of oxide on said bottom of said well;

5) wet etching said nitride off said vertical walls of said well to expose said pad oxide;

6) growing said self aligned floating gate insulating material layer only on said vertical walls of said well since the bottom of said well is already covered by an oxide layer and a top surface of said substrate is also already covered by an oxide layer;

7) depositing a layer of doped polysilicon conductor over said substrate and into said well to cover said vertical walls and bottom of said well;

8) ***forming a self aligned floating gate without using a critical mask by etching back said doped polysilicon from all horizontal surfaces thereby removing all doped polysilicon from a top surface of said oxide layer which covers said top surface of said substrate and said bottom of said vertical well and leaving doped polysilicon on all vertical walls of said well***, where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit;

9) forming a layer of silicon dioxide insulator covered by a layer of nitride insulator covered by another layer of silicon dioxide insulator (hereafter ONO) over said oxide layer covering said top surface of said substrate, said ONO layer extending down into said vertical well and covering said self aligned floating gate;

10) depositing over said ONO layer a second layer of doped polysilicon conductor from which said self aligned control gate will be formed;

11) growing a layer of oxide over said second layer of doped polysilicon;

12) using a non critical mask to etch away portions of said second layer of doped polysilicon to define lateral extents of said self aligned control gate above said top surface of said substrate leaving said layer of oxide on a top surface of said control gate;

13) depositing a layer of oxide over said surface of said substrate and covering said control gate's vertical side walls;

14) anisotropically etching back said layer of oxide deposited in step 13 to remove oxide only from horizontal surfaces and leaving spacer oxide only on vertical side walls of said polysilicon of said control gate and word line thereby defining outer edges of said spacer oxide layer where said outer edges are edges of said spacer oxide layer which are farthest from a centerline of said well in a direction along said long axis of said row;

15) using a non critical mask to define the lateral extents of contact holes to said drain region etching through said ONO layer formed in step 9 and said oxide layer covering said top surface of said substrate to self align said ONO layer to the lateral extents of said [spacer oxide layer defined in step 14] control gate and leave two contact holes to said drain regions adjacent to said two side of said well which are orthogonal to said long axis of said row of nonvolatile memory cells in said array of nonvolatile memory cells, said contact holes being self aligned to said outer edges of said spacer oxide layer.

15. [Once Amended-Version To Show Changes] In a vertically integrated nonvolatile memory cell structure formed using a vertical well that penetrates doped drain and channel regions and into a source region of a substrate, said vertical well having a top edge and a bottom, a self aligned floating gate insulating layer substructure comprising:

a self aligned floating gate insulating material layer on [the] all vertical walls of said well and which does not extend above the top of said well; and

an insulating layer on the bottom of said well.

16. The self aligned floating gate insulating material substructure of claim 15 manufactured by a process which does not use any critical mask in the steps used to form said self aligned floating gate insulating material layer such that it does not extend above said top of said well , where a critical mask is defined as a mask which requires close alignment to registration marks so as to cause close alignment between different structures on an integrated circuit[, where a critical mask is defined as a mask which is required for tight tolerance alignment between different layers of a semiconductor structure].

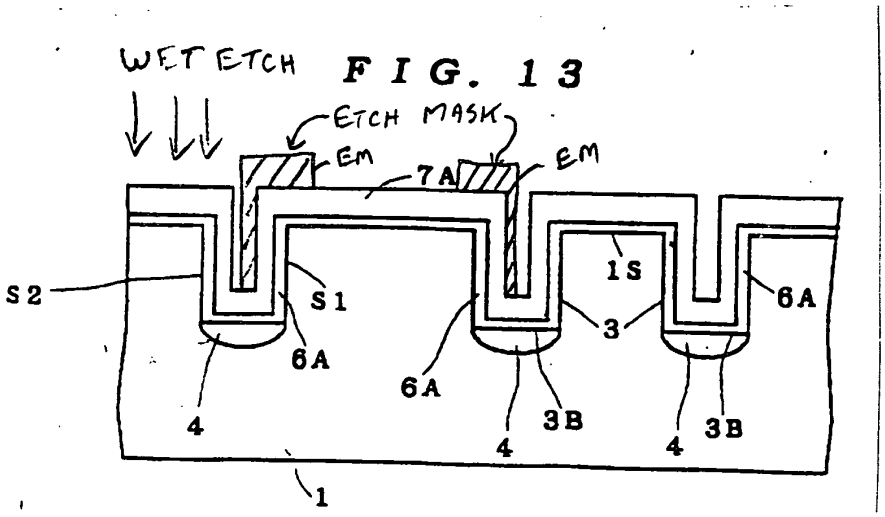
WET ETCH
FIG. 13
ETCH MASK
EM
7A
EM
1S
S2
S1
6A
3
6A
6A
4
3B
4
4
3B
1

FIG. A-1

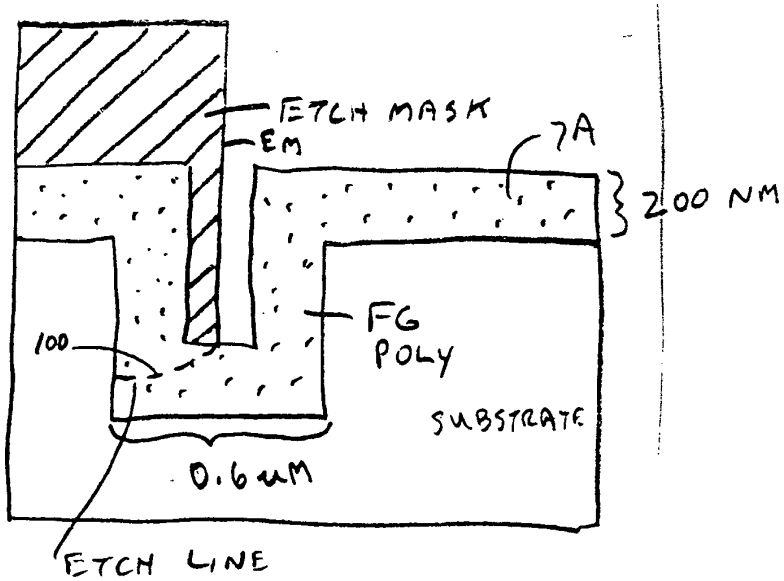
ETCH MASK
EM
7A
200 NM
FG
POLY
100
SUBSTRATE
0.6 μM
ETCH LINE

FIG. A-2

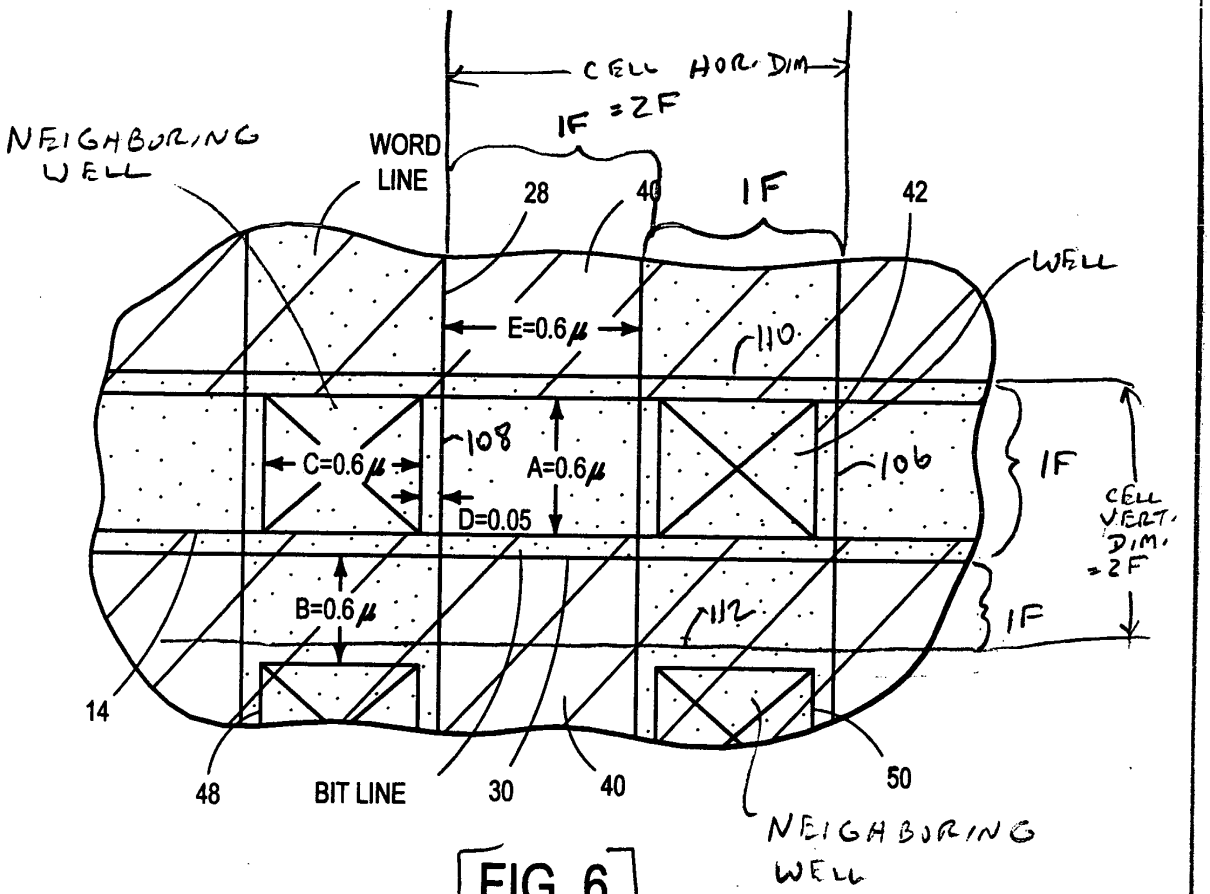

FIG. 6

TOTAL AREA $4F^2$

FIG. A-5

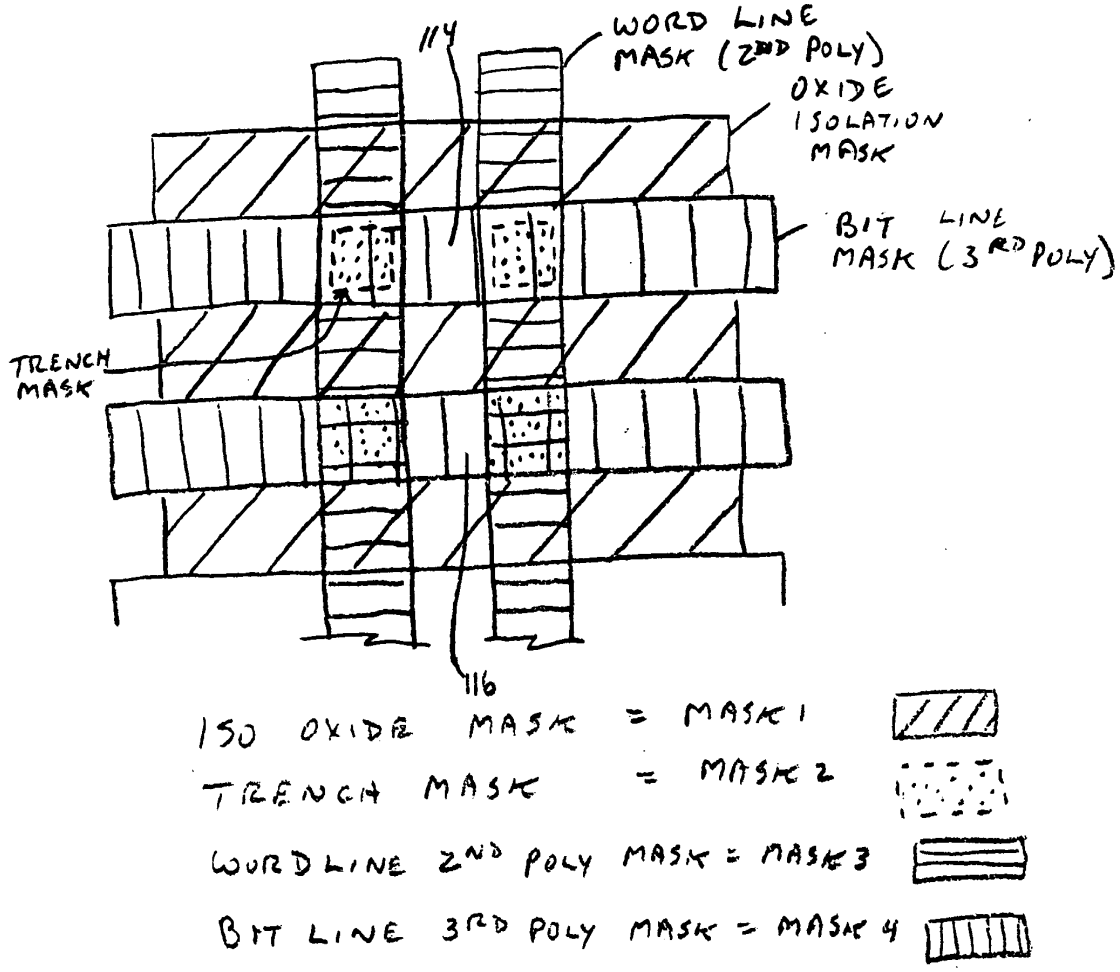
114
WORD LINE MASK (2ND POLY)
OXIDE ISOLATION MASK
BIT LINE MASK (3RD POLY)
TRENCH MASK
116
ISO OXIDE MASK = MASK 1
TRENCH MASK = MASK 2
WORDLINE 2ND POLY MASK = MASK 3
BIT LINE 3RD POLY MASK = MASK 4

FIG. A-6

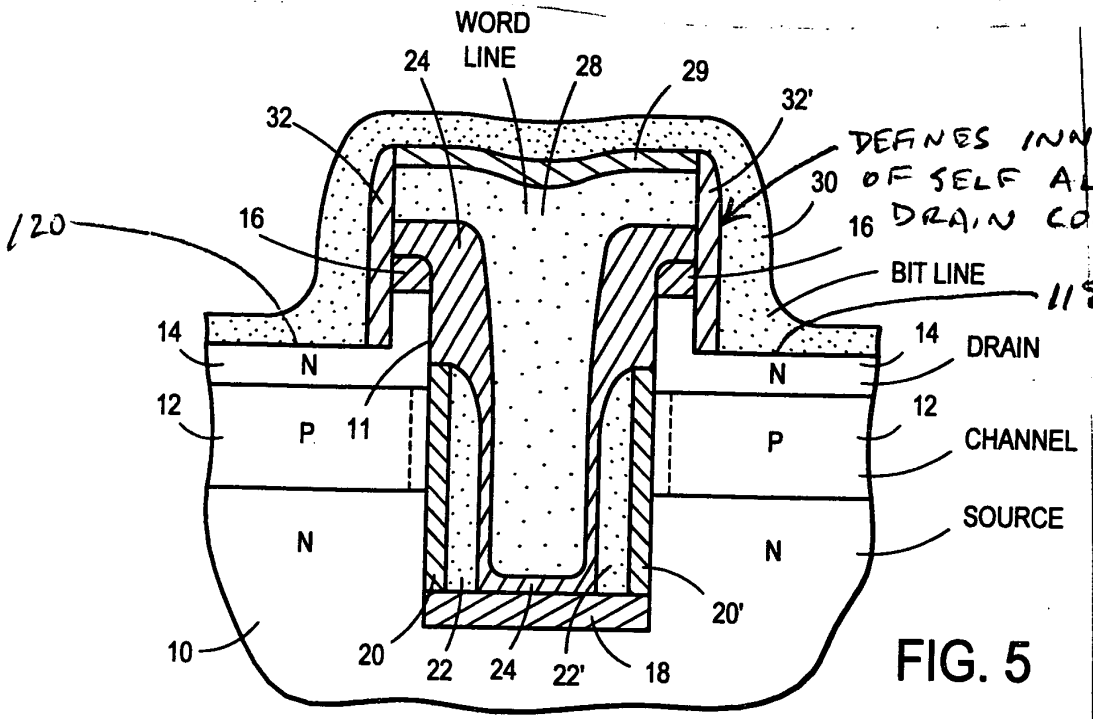

FIG. 5

COMPLETED DEVICE OF INVENTION

FIG. A-7

FIG. 23

(FROM OTANI ET AL. 5,786,612)

CELL SIZE 2F x 4F = 8F²

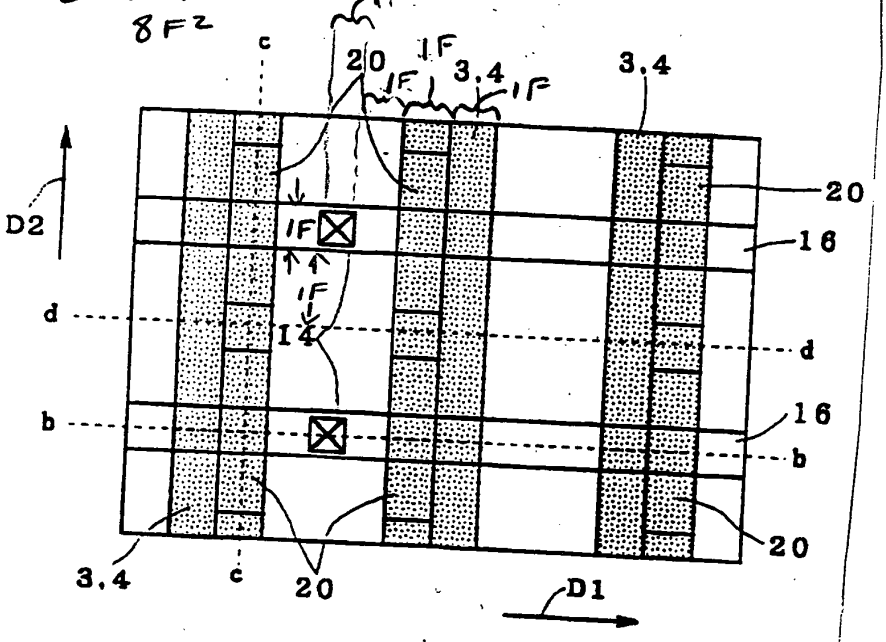

FIG. A-8

EXHIBIT A
P. 4